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A TWO STEP TRENCH DEFINITION PROCEDURE FOR FORMATION OF A DUAL DAMASCENE OPENING IN A STACK OF INSULATOR LAYERS

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to methods used to fabricate semiconductor devices, and more specifically to a method used to form a dual damascene opening in a stack of insulator layers to expose an underlying conductive gate structure.

(2) Description of the Prior Art

Dual damascene openings formed in insulator layers has enabled conductive via structures as well as overlying conductive interconnect structures to be defined simultaneously in the dual damascene opening. One method of forming a dual damascene opening is to first define a narrow diameter via opening in an entire stack of insulator layers, exposing a top surface of an underlying conductive interconnect structure, followed by definition of a wider diameter trench shape in a top portion of the same insulator layer stack. The above procedure can however result in damage to the top surface of the exposed underlying conductive interconnect structure during the trench definition procedure, resulting in possible higher than desired interface resistance when overlaid with an conductive via structure. In addition other dual damascene opening

procedures can also result in loss of insulator thickness as well as corner rounding of the exposed top insulator component of the via opening occurring during various stages of the definition procedure.

The present invention will describe a procedure for formation of a dual damascene opening in a stack of insulator layers in which a critical process step, the step used to remove all stop or liner layers, is accomplished using a two step removal sequence which reduces the risk of corner rounding of an top insulator layer, as well as reducing the risk of damage to an exposed underlying conductive interconnect structure. In addition to the novel two step stop layer removal procedure the present invention will describe etch chemistries and selectivities which also reduce the risk of damage to the underlying conductive interconnect structure during the dual damascene opening procedure. Prior art such as Liu et al, in U.S. Pat. No. 6,211,063 B1, as well as Moise et al, in U.S. Pat. No. 6,211,035 B1, describe methods of forming self aligned conductive structures in a dual damascene opening, as well as simultaneously forming openings to multiple conductive structures located at various levels. These prior art however do not describe the novel process sequence and etch chemistry employed in the present invention for dual damascene openings in an insulator stack in which corner rounding, loss of top insulator layer thickness, as well as damage to an exposed underlying conductive structure, is reduced as a result of the two step stop layer removal procedure.

SUMMARY OF THE INVENTION

It is an object of this invention to form a dual damascene opening in a stack of insulator layers to expose a top surface of an underlying conductive structure.

It is another object of this invention to employ a two step, dry etching procedure in the dual damascene opening procedure for removal of the stop or liner layers used as components in the stack of insulator layers, to reduce the risk of corner rounding of a capping insulator layer component of the stack of insulator layers.

It is still another object of this invention to employ the two step, dry etching procedure in the dual damascene procedure for removal of the stop or liner layers used as components of the stack of insulator layers, to reduce the risk of damage to the top surface of an underlying conductive structure, exposed at the dual damascene opening at the conclusion of the dual damascene opening procedure.

In accordance with the present invention a process of defining a dual damascene opening in a stack of insulator layers featuring a two step dry etching procedure, used for removal of stop or liner layer components of the insulator stack, is described. A stack of insulator layers comprised of; underlying silicon nitride stop or liner layer, a fluorinated silica glass layer, an overlying silicon nitride stop or liner layer, an overlying silicon oxide layer, an anti-reflective coating layer, and a silicon oxide capping layer, is formed on an underlying conductive structure. A first photoresist shape is used for definition of a narrow diameter via opening in the stack of

insulator layers, with the via opening component of the dual damascene opening terminating within the underlying silicon nitride stop layer. Formation of second photoresist shape fills the narrow diameter opening, with the second photoresist shape comprised with a trench shape opening exposing portions of the top surface of the silicon oxide capping layer. A dry etch procedure is employed to allow the trench shape of the dual damascene opening procedure to be defined in top components of the insulator stack, with the trench definition procedure terminating at the appearance of the top surface of the overlying silicon nitride stop layer, with the dry etch procedure also resulting in the formation of a photoresist plug located in a bottom portion of the narrow diameter via opening. With the photoresist plug protecting underlying materials a first phase of the two step dry etching procedure is initiated removing the portion of the overlying silicon nitride stop layer exposed in the trench opening. After removal of the photoresist plug a second phase of the two step dry etch procedure is employed to selectively remove the portion of the partially etched, underlying silicon nitride stop layer exposed at the bottom of the via opening, resulting in exposure of a portion of a top surface of the underlying conductive structure.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the preferred embodiments with reference to the attached drawings that include:

Figs. 1 - 7, which schematically in cross - sectional style show key stages used to define a

dual damascene opening in a stack of insulator layers, featuring a two step procedure employed for removal of the stop or liner layer components of the insulator stack.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The method of defining a dual damascene opening in a stack of insulator layers, featuring a two step procedure employed for removal of the stop or liner layer components of the insulator stack, will now be described in detail. Conductive structure 2, a structure comprised of a material such as a copper, is shown schematically shown in Fig. 1, embedded in insulator layer 1, wherein insulator layer 1, can be comprised of silicon oxide, or a boro-phosphosilicate glass (BPSG). First liner or stop layer 3, a layer such as silicon nitride, is deposited to a thickness between about 400 to 600 Angstroms via plasma enhanced chemical vapor deposition (PECVD) procedures. Insulator layer 4, a fluorinated silica glass (FSG) layer, is next formed on first liner layer 3, at a thickness between about 250 to 1000 Angstroms via PECVD procedures. Second liner layer 5, again a layer such as silicon nitride, is next deposited to a thickness between about 200 to 400 Angstroms via PECVD procedures. Insulator layer 6, comprised of silicon oxide, is deposited on second silicon nitride layer 5, at a thickness between about 500 to 1000 Angstroms via PECVD procedures. Anti-reflective coating (ARC) 7, a layer such as silicon oxynitride, is next formed on insulator layer 6, at a thickness between about 500 to 700 Angstroms, via PECVD or physical vapor deposition (PVD) procedures, followed by deposition of capping oxide layer 8, a silicon oxide layer, formed to a thickness between about 500 to 700 Angstroms via PECVD procedures. The result of these procedures is schematically shown in Fig. 1.

First photoresist shape 9, is next employed to allow an anisotropic reactive ion etching (RIE), procedure to define narrow diameter, via opening 10, in capping oxide layer 8, in ARC layer 7, in insulator layer 6, in second liner layer 5, and in FSG layer 4, with the anisotropic RIE procedure terminating in a top portion of first liner layer 3. The anisotropic RIE procedure is performed using CHF_3 as an etchant for capping oxide layer 8, insulator layer 7, ARC layer 6, and for FSG layer 4, while either CF_4 or CH_xF_y is used as a selective etchant for silicon nitride, second liner layer 5. The diameter of via opening 10, is between about 0.25 to 2.5 um. The result of the above via opening definition procedure is schematically shown in Fig. 2.

The procedure used to form a photoresist plug in a bottom portion of via opening 10, as well as to form a trench opening in a top portion of the insulator stack is next addressed and schematically illustrated in Figs. 3 - 4. Photoresist shape 12a, shown schematically in Fig. 3, is next formed completely filling via opening 10, with photoresist shape 12a, featuring trench shape opening 13, which exposes a portion of the top surface of capping oxide layer 8. A dry etch procedure employed to form the trench shape of the dual damascene opening, and to form a photoresist plug at the bottom of the narrow diameter via opening of the dual damascene opening in next addressed. A selective, anisotropic RIE procedure performed using CHF_3 as an etchant, is employed to transfer or define trench opening 13, in underlying insulator layers, specifically defining trench shape 13, in capping oxide layer 8, in ARC layer 7, and in insulator layer 6, with the anisotropic RIE procedure selectively terminating at the appearance of second liner layer 5, comprised of silicon nitride. The same anisotropic RIE procedure results in an etch back of the portion of photoresist shape 12a, located in narrow diameter via opening 10, resulting in the

formation of photoresist plug 12b, in the bottom portion of via opening 10, wherein photoresist plug 12b, is located overlying a portion of the top surface of conductive structure 2. This is schematically shown in Fig. 4. The top surface of photoresist plug 12b, is located below the bottom surface of second liner layer 5.

With second photoresist shape 12a., and with photoresist plug 12b, in place, the first of the two step liner removal procedure is performed. A selective RIE procedure using CF_4 or CH_xF_y as a selective etchant for the portions of second liner layer exposed in trench shape opening 13, is performed featuring selective termination of the RIE procedure on the top surface of, or in a top portion of FSG layer 4. Photoresist plug 12b, located on a portion of first liner layer 3, protected silicon nitride, first liner layer 3, during the first stage of the two step liner removal procedure. This is schematically shown in Fig. 5. The selectivity of the RIE procedure resulted in only between about 50 to 150 Angstroms of thinning of FSG layer 4, during the first step of the two step liner removal procedure. In addition the presence of photoresist shape 12a, prevented unwanted corner rounding of capping oxide layer 8.

Removal of photoresist shape 12a, and of photoresist plug 12, is next accomplished via plasma oxygen ashing procedures, resulting in exposure of partially etched first liner layer 3, located in at the bottom of via opening 10. This is schematically shown in Fig. 6. Another selective RIE procedure is employed to remove the portion of first liner layer 3, exposed in via opening 10. The selective RIE procedure is accomplished using CF_4 or CH_xF_y as an etchant for the silicon nitride first liner layer, with an etch rate ratio of silicon nitride to either FSG or silicon

oxide of about between about 5 to 1, to 10 to 1. The etch rate ratio or etch rate selectivity for the first liner removal procedure resulted in only a minimum of FSG removal, between about 50 to 100 Angstroms, and removal of only between about 50 to 100 Angstroms of capping oxide layer 8. In addition the selective RIE first liner layer removal procedure did not result in rounded corners at the top surface of capping oxide layer 8, nor did damage occur to the top surface of conductive structure 2, at conclusion of the selective RIE first liner layer removal procedure. The result of this procedure, featuring dual damascene opening 14, comprised of trench opening 13, and via opening 10, exposing a portion of the top surface of conductive structure 2, is schematically shown in Fig. 8.

While this invention has been particularly shown and described with reference to, the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of this invention.

What is claimed is: